IN THE CLAIMS:

Please amend the claims as follows:

Claims 1-16 (Cancelled)

Claim 17 (NEW): A coding cell of a nonvolatile ferroelectric memory device, comprising:

a first latch having one node connected with a first node and the other node connected with second and third nodes;

a first transistor having a gate terminal to which a gate control signal is input, a source terminal to which a signal of the second node is transferred, and a drain terminal to which a first data signal is input;

a second transistor having a gate terminal to which the gate control signal is input, a source terminal to which a signal of the third node is transferred, and a drain terminal to which a second data signal is input;

a second latch having one node connected with a fourth node and the other node connected with the second and third nodes;

a first ferroelectric capacitor arranged between an input terminal of a control signal and the second node;

a second ferroelectric capacitor arranged between the input terminal of the control signal and the third node;

a third ferroelectric capacitor arranged between the second node and a voltage terminal; and

a fourth ferroelectric capacitor arranged between the third node and the voltage terminal.

Claim 18 (NEW): The coding cell of claim 17, further comprising an equalizing block between the second and third nodes.

Claim 19 (NEW): The coding cell of claim 17, further comprising a switching block operating in response to signals of the second and third nodes.

Claim 20 (NEW): A coding cell of nonvolatile ferroelectric memory device, comprising:

a PMOS transistor transferring a power source voltage VCC to a first node in response to a first control signal;

a first latch having one node connected with the first node and the other node connected with second and third nodes;

a first transistor having a gate terminal to which a gate control signal is input, a source terminal to which a signal of the second node is transferred, and a drain terminal to which a first data signal is input;

a second transistor having a gate terminal to which the gate control signal is input, a source terminal to which a signal of the third node is transferred, and a drain terminal to which a second data signal is input;

a third transistor transferring a ground voltage VSS to a fourth node in response to a second control signal;

a second latch having one node connected with the fourth node and the other node connected with the second and third nodes;

a switching block operating in response to signals of the second and third nodes;

a first ferroelectric capacitor arranged between an input terminal of a third control signal and the second node;

a second ferroelectric capacitor arranged between the input terminal of the third control signal and the third node;

a third ferroelectric capacitor arranged between the second node and a voltage terminal; and

a fourth ferroelectric capacitor arranged between the third node and the voltage terminal.

Claim 21 (NEW): The coding cell of claim 20, further comprising an equalizing block between the second and third nodes.

Claim 22 (NEW): The coding cell of claim 20, further comprising a switching block operating in response to signals of the second and third nodes.

Claim 23 (NEW): A method for operating a coding cell of a nonvolatile ferroelectric memory device having first and second nodes between two latches, a first ferroelectric capacitor arranged between an input terminal of a control signal and the first node, a second ferroelectric capacitor arranged between the input terminal of the control signal and the second node, a third ferroelectric capacitor arranged between the first node and a voltage terminal, and a fourth ferroelectric capacitor arranged between the second node and the voltage terminal, comprising:

sensing a voltage difference from first and second data stored in the first and second ferroelectric capacitors in response to power-up sensing pulse during a power-up mode;

restoring the first data in the first ferroelectric capacitor in case of the control signal of logic "high" level, and restoring the second data in the second ferroelectric capacitor in case of the control signal of logic "low" level.

Claim 24 (NEW): A method for operating a coding cell of a nonvolatile ferroelectric memory device having first and second nodes between two latches, a first ferroelectric capacitor arranged between an input terminal of a control signal and the first node, a second ferroelectric capacitor arranged between the input terminal of the control signal and the second node, a third ferroelectric capacitor arranged between the first node and a voltage terminal, and a fourth ferroelectric capacitor arranged between the second node and the voltage terminal,

wherein a first data is stored in the first ferroelectric capacitor or the second ferroelectric capacitor in case of a gate control signal of logic "high" level and the control signal of logic "high" level during a write program mode, and a second data is stored in the first ferroelectric capacitor or the second ferroelectric capacitor in case of the gate control signal of logic "low" level and the control signal of logic "low" level.